Detector needs for synchrotron diffraction techniques

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Area Detectors
Fundamentals - Counting versus Integrating

Analog Output
• Pulse Height ~ Energy

τ ~ 100 ns
Area Detectors

Fundamentals - Counting versus Integrating

Analog Output
- Pulse Height ~ Energy

? ~ 100 ns

Counting
“digital” (e.g., Pilatus)
Area Detectors
Fundamentals - Counting versus Integrating

Counting
“digital”
(e.g., Pilatus)

Integrating
“analog”
(e.g., CCDs)

Analog Output
- Pulse Height ~ Energy

\[ \tau \sim 100 \text{ ns} \]

Digitizer
Dark Current

“digital”
“analog”
Area Detectors
From analog to digital

CCDs (integrating/analog, slow)
Area Detectors
From analog to digital

CCDs (integrating/analog, slow)

Counting pixel array detectors (counting/digital, fast, but…)
Pixel Detectors
Integrated Circuits (ASIC, ROIC)

Direct Detection of X-rays in solid state sensor
→ Point Spread Function: < 1 pixel

3.6 eV to create 1 eh-pair @12keV: 3300 eh-pairs
Pixel Detectors
CMOS Integrated Circuits (ASIC, ROIC)

ASIC = Application Specific Integrated Circuit
ROIC = Readout Integrated Circuit
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Area Detectors
Photon counting, speed and dynamic range

Pilatus specs
- 487 x 195 pixels (172 microns)
- Count Rate ~ 1 MHz/pixel
- 20-bit counter/pixel
- Frame Rate = 200 Hz
- Gateable & electronic shutter
- Lower Level Discriminator only

You do not have 20-bit dynamic range @ 200 Hz!!!

<table>
<thead>
<tr>
<th>Frame Rate (Hz)</th>
<th>Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Hz</td>
<td>$10^6$ (20-bits)</td>
</tr>
<tr>
<td>10 Hz</td>
<td>$10^5$</td>
</tr>
<tr>
<td>100 Hz</td>
<td>$10^4$</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1</td>
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</tbody>
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Dynamic range decreases with frame rate!
Area Detectors – analog is back!

Integrating detectors are needed for both high dynamic range & speed

- There are a number of R&D projects working on charge integrating detectors
  - Photon counting detector are much easier to realize.

- **Mixed-Mode PAD (Cornell/APS/Sydor)**
  - Remove discrete amounts of charge and count (Not for XFELs or serial crystallography)
  - Dynamic range ~ $10^8$
  - ~ 1 kHz frame rate; 150 µm pixels
  - Silicon being commercialized via Sydor and CdTe version under development.

- **JUNGFRAU (PSI for SwissFEL/SLS)** (SLAC ePix10k is similar but 100 µm pixel)
  - Adaptive gain switch (XFEL or serial crystallography compatible)
  - Dynamic range ~ $10^4$
  - ~ 1 kHz frame rate; 75 µm pixels
  - Only Silicon, right now.

- **AGIPD (EU-XFEL)**
  - 352 images at 4.5 MHz in burst mode
  - 200 µm pixels
  - $10^4$ dynamic range per image
  - DESY/X-spectrum is willing to sell a Silicon version and working on a GaAs version for XFEL HiBEF.
  - Cornell also has similar development called Keck PAD (currently has SBIR funding), except 8 images only.
How do we move from kHz to MHz (continuous)?
Burst-mode MHz frame rate detectors exist

Keck, AGIPD, LPD, DSSC, UXI, FASPAX, etc

Keck PAD (CU) ~ 10 MHz, 12 images

AGIPD (EU-XFEL) ~ 5 MHz, 352 images

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High-speed X-ray imaging pixel array detector for synchrotron bunch isolation

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A wide dynamic range imaging X-ray detector designed for recording successive frames at rates up to 10 MHz is described. X-ray imaging with frame rates of up to 6.5 MHz have been experimentally verified. The pixel design allows for up to 8-12 frames to be stored internally at high speed before readout, which occurs at a 1 kHz frame rate. An additional mode of operation allows the integration capacitors to be re-addressed repeatedly before readout which can enhance the signal-to-noise ratio of cyindrical processes. The detector, along with modern storage ring sources which provide short (10-100 ps) and intense X-ray pulses at megahertz rates, opens new avenues for the study of rapid structural changes in materials. The detector consists of hybridized modules, each of which is comprised of a 500 µm-thick silicon X-ray sensor solder bump-bonded, pixel by pixel, to an application-specific integrated circuit. The format of each module is 128 x 128 pixels with a pixel pitch of 150 µm. In the prototype detector described here, the three-side battable modules are tiled in a 3 x 2 array with a full format of 256 x 384 pixels. The characteristics, operation, testing and application of the detector are detailed.

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200 µm

Analog Memory 352 cells

Analog front end

Analogue value capacitor

Memory cell switches

Gain bit capacitor

(b) Pixel layout.
Burst-mode MHz frame rate detectors exist
Analog front-ends are sufficiently fast!

AGIPD (EU-XFEL) ~ 5 MHz, 352 images

Figure 3. MPW prototypes and a fullscale ASIC.
How to move to CW MHz?

Move to a digital-dominated design with sub-100nm CMOS

AGIPD (130 nm CMOS)
Most of pixel is storage (burst)

Old approach: analog-dominated; design 1 pixel; step & repeat identical copies; custom made digital (if any at all)
How to move to CW MHz?
Move to a digital-dominated design with sub-100nm CMOS

**New approach**
- The big gain in sub-100nm CMOS is in the digital domain (clock speed and logic density).
- Going to smaller process nodes is the most effective path to high logic density.
  - CMOS feature size reduction results to first order in a quadratic increase with feature reduction factor.
- Transmission rates of digital data can be higher than analog data and use standardized interfaces.
- Digital signals are less prone to corruptions; error detection and correction algorithms can ensure data integrity.
- Digital data manipulation can be incorporated, such as on-chip compression schemes

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(b) Pixel layout.
How to move to CW MHz?
In-pixel digitization, move data to edge & maximize off-chip bandwidth

AGIPD (130 nm CMOS)
Most of pixel is storage (burst)

**New approach:** Instead of using pixel area for storage, use it to transmit digital data to the edge (more room). Synthesized entire design with analog IP in a hierarchical way.

Digital-dominated design

In-pixel ADC and high-speed daisy-chained digital data path. Wide and fast data buses allow high-speed transfer of event data to chip edge for processing and transmission off chip.)
High-speed readout (off-chip)

Simple math

• \((256\times256\ \text{pixels}) \times (16\ \text{bits}) \times (200\ \text{kHz}) = 200\ \text{Gbps}\)
• \((256\times256\ \text{pixels}) \times (16\ \text{bits}) \times (1\ \text{MHz}) = 1\ \text{Tbps}\)

Three ways to get data off the chip as fast as possible
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Three ways to get data off the chip as fast as possible

1. High-speed transceivers
   - In 65 nm, 10 Gbps is possible, but challenging
   - CERN’s lpGBT (Power ~ 0.5W!!)
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Three ways to get data off the chip as fast as possible

1. **High-speed transceivers**
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2. **Multiple high-speed transceivers**
   • In 65 nm, 10-20 10 Gbps might be possible one chip \(\rightarrow\) 100-200 Gbps
     • Timepix-4 is attempting 16 x 10 Gbps links
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3. **Compress data before you send off the chip**
   - “Bandwidth compression”
   - Compression exploits smoothness, autocorrelation and recurring patterns
How to move to CW MHz?

On-chip compression (i.e., “bandwidth compression”)

• Making the most efficient use of limited off-chip bandwidth will increase frame rates
• Digital-dominated designs make it straightforward to incorporate algorithms (once translated into RTL).
  • LZ4 lossless compressor block ~ 400k gates
    (doi:10.1587/elex.14.20170399, area ~ 0.3 mm x 1.7 mm in 65 nm)
• Lossless compression ratios
  • ~ 10 for macromolecular diffraction datasets (lz4-bs)
  • ~ 15 for ptychography datasets (Zstd) (Junjing Deng et al)
• “Scientific” lossy (SZ) compressor ratios (doi:10.1109/BigData.2018.8622520)
  • ~ 20 for a crystallography application (LCLS data)
    (doi:10.1177/1094342019853336)
• Can we live with some lossy compression? Reconstructions?
  • Compression more lossy where there less information?
On-chip compression (i.e., “bandwidth compression”)

First steps at Argonne

- Working in collaboration with ANL computing division (MCS) on ASIC compressor designs (Yoshii, Cappello, et al)
Strategies for on-chip data compression for charge integrating pixel detectors

Compression in the pixel

Digital lower threshold ("de-noiser") and conversion from ADUs to photons

Analog Front End

12-bit ADC

digital register

adder

12-bit divider

offset 3

divisor 3

gain

daisy chained data to following pixel columns

116\text{\mu m} \times 116\text{\mu m}

Digital Logic divider and de-noiser
35\text{\mu m} \times 100\text{\mu m}

ADC and Front End
65\text{\mu m} \times 90\text{\mu m}

Additional Logic

100\text{\mu m} \text{excluding power rings}

daisy chained signals between abutted pixel columns
Strategies for on-chip data compression for charge integrating pixel detectors

Compression at the detector ASIC periphery

A simple, lossless delta encoding scheme gives compression ratio of ~ 10 for Pilatus ff-HEDM dataset.
Beyond Silicon Sensors

> 20keV
Beyond Silicon Sensors

Beyond 20 keV…. CdTe, GaAs, Ge, etc?

![Graph showing X-ray absorption efficiency for Si, GaAs, CdTe, and Ge](Image)

**Graph Details:**
- **X-axis:** Photon energy / keV
- **Y-axis:** Fraction of absorbed intensity
- **Legend:**
  - 300 μm Si
  - 700 μm Si
  - 1 mm Si
  - 500 μm GaAs
  - 1 mm CdTe
  - 2 mm CdTe
  - 3000 microns Ge
Beyond Silicon Sensors
Beyond 20 keV.... CdTe, GaAs, Ge, etc?

CdTe gain variations after *moderate* dose for the MM-PAD detector at 0 C.

(a) Before dosing.  (b) After exposure to $3 \times 10^{11}$ photons/mm$^2$.

Compound semiconductors are unlikely to be perform well under high dose conditions (e.g., XFELs or high-flux synchrotrons experiments) due to high crystal defects.

https://arxiv.org/abs/1609.03513
Summary

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  - Will allow for more digital logic in the detector chip such as compression, auto-calibration
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- CW MHz frame rates are within reach with modern sub-100nm CMOS integrated circuit technology
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- Sensors beyond silicon are a big material science problem!
  - Integrating detectors will not “hide” the problem like the Pilatus CdTe!
Extra slides
Custom ptychographic processing units?
Near-detector, real-time AI computing for high-throughput lensless imaging

- Various forms of X-ray lenless image reconstruction through backpropagation have been implemented in Tensorflow (Youssef S.G.Nashed et al).
- One can imagine some sort of TPU-like architecture with additional FFT-specific capabilities would be very useful for those algorithms.